Filed electronically on March 17, 2008 *PATENT*
Dkt. STL11280

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: **Wayne L. Felts**
Assignee: **SEAGATE TECHNOLOGY LLC**
Application No.: **10/606,090** Group Art Unit: **2116**
Filed: **June 26, 2003** Examiner: **James Trujillo**
For: **TRANSITIONING FROM STARTUP CODE TO APPLICATION CODE DURING INITIALIZATION OF A PROCESSOR BASED DEVICE**

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P. O. Box 1450
Alexandria, Virginia 22313-1450

ATTENTION: Board of Patent Appeals and Interferences

Sir:

APPELLANT'S BRIEF

This Brief is in furtherance of the Notice of Appeal filed concurrently herewith. A first Appeal Brief was filed July 12, 2007, and a new non-final Office Action was mailed October 12, 2007 responsive to this first Brief. The Applicant has accordingly elected to file a new appeal under 37 CFR 41.37, with the previously paid notice of appeal fee and appeal brief fee being applied to this new appeal. 37 CFR 41.20, 41.37.

The required fees, petition for extension of time for filing this Brief, and the authority and time limits established by the Notice of Appeal are dealt with in the accompanying TRANSMITTAL OF APPEAL BRIEF.

This brief contains these items under the following headings, and in the order set forth below:

I. REAL PARTY IN INTEREST
II. RELATED APPEALS AND INTERFERENCES
III. STATUS OF CLAIMS

I. REAL PARTY IN INTEREST

The real party in interest in this Appeal is Seagate Technology LLC.

II. RELATED APPEALS AND INTERFERENCES

There are no other appeals or interferences that will directly affect, or be directly affected by, or have a bearing on the Board's decision in this Appeal.

III. STATUS OF CLAIMS

The status of the claims in this application is:

Claim	Status
1. (Original)	Independent.
2. (Original)	Depends from claim 1.
3. (Original)	Depends from claim 1.
4. (Original)	Depends from claim 3.
5. (Original)	Depends from claim 4.
6. (Original)	Depends from claim 1.
7. (Original)	Depends from claim 6.
8. (Previously presented)	Independent.
9. (Original)	Depends from claim 8.
10. (Original)	Depends from claim 8.
11. (Original)	Depends from claim 10.
12. (Original)	Depends from claim 8.
13. (Original)	Depends from claim 12.
14. (Previously presented)	Independent.
15. (Original)	Depends from claim 14.
16. (Original)	Depends from claim 14.
17. (Original)	Depends from claim 14.
18. (Original)	Depends from claim 17.
19. (Previously presented)	Depends from claim 1.
20. (Previously presented)	Depends from claim 1.

A. TOTAL NUMBER OF CLAIMS IN APPLICATION

Claims in the application: 1-20.

B. STATUS OF ALL THE CLAIMS

1. Claims canceled: None.
2. Claims withdrawn from consideration but not canceled: None.
3. Claims pending: 1-20.
4. Claims allowed: None.
5. Claims rejected: 1-20.
6. Claims objected to: None.

C. CLAIMS ON APPEAL

Claims now on appeal: 1-20.

IV. STATUS OF AMENDMENTS

No post-final amendments have been submitted.

V. SUMMARY OF CLAIMED SUBJECT MATTER

The embodiments of the present invention as recited by the language of independent claims 1, 8 and 14 are generally directed to an apparatus and method for processor control of an electrical load.

Independent claim 1 generally features a method comprising controlling an electrical load (such as 106, 116 in FIG. 1) with a first code (such as in "BOOT ROM" 136, FIG. 3 and "MEM 1" 220 in FIG. 8) executed by a processor (such as 132 in FIG. 3) – see steps 1-2 in FIG. 8; step 254 in FIG. 9; and in the specification at page 11, lines 1-8 and page 15, lines 4-7. The method of claim 1 further generally comprises releasing processor control so that the

electrical load operates in an open control mode while the first code is displaced with a second code (such as in "RAM" 134, FIG. 3 and "MEM 2" 222 during step 2 of FIG. 8) – see step 3 in FIG. 8; step 258 in FIG. 9; and in the specification at page 10, lines 16-23; page 11, lines 20-25; and page 15, lines 9-11. The method of claim 1 further generally comprises reinstating processor control of the electrical load using the second code – see step 4 in FIG. 8; step 260 in FIG. 9; and in the specification at page 11, lines 26-31; page 13, lines 24-28; page 15, lines 11-14; page 16, lines 16-21.

Independent claim 8 generally features a method comprising using a processor (such as 132 in FIG. 3) to execute startup code (such as in "BOOT ROM" 136, FIG. 3) loaded into a memory location (such as "MEM 1" 220 in FIG. 8) to initiate operational control of an electrical load (such as 106, 116 in FIG. 1) – see steps 1-2 in FIG. 8; step 254 in FIG. 9; and in the specification at page 11, lines 1-8 and page 15, lines 4-7. The method of claim 8 further generally comprises continuing to operate the electrical load while processor operational control of the electrical load is temporarily suspended to load application code (such as from "MEM 2" 222, FIG. 8) to the memory location ("MEM 1" 220, FIG. 8) – see step 3 in FIG. 8; step 258 in FIG. 9; and in the specification at page 10, lines 16-23; page 11, lines 20-25; page 15, lines 9-11; and page 16, lines 22-25. The method of claim 8 further generally comprises resuming operational control of the electrical load using the application code - see step 4 in FIG. 8; step 260 in FIG. 9; and in the specification at page 11, lines 26-31; page 13, lines 24-28; and page 15, lines 11-14.

Independent claim 14 generally features an apparatus comprising an electrical load (such as 106, 116 in FIG. 1); a memory location (such as "MEM 1" 220 in FIG. 8); and a programmable processor (such as 132, FIG. 3) coupled to the memory location and adapted

to control the electrical load, wherein during an initialization process (such as 250, FIG. 9) the processor executes startup code loaded into the memory location to initiate operational control of the load (such as steps 1-2 in FIG. 8 and step 254, FIG. 9) – see specification at page 11, lines 1-8 and page 15, lines 4-7. The processor further temporarily releases operational control of the electrical load so that the electrical load continues to operate in an open control mode while application code is loaded to the memory location (such as step 3 in FIG. 8 and step 258, FIG. 9) – see specification at page 10, lines 16-23; page 11, lines 20-25; page 15, lines 9-11; and page 16, lines 16-25. The processor further resumes operational control of the electrical load using the application code (such as step 4 in FIG. 8 and step 260, FIG. 9) – see specification at page 11, lines 26-31; page 13, lines 24-28; and page 15, lines 11-14.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

1. The rejection of claims 1-2, 6-7 and 19-20 under 35 U.S.C. §103(a) as being obvious over U.S. Published Patent Application No. US2004/0019776A1 to Sato et al. ("Sato '776") in view of U.S. Published Patent Application No. US2002/0167287A1 to Heydt et al. ("Heydt '287") is presented as a first grounds of rejection to be reviewed on appeal.

2. The final rejection of claims 3-5 and 8-18 under 35 U.S.C. §103(a) as being obvious over Sato '776 and Heydt '287, further in view of U.S. Patent No. 6,405,311 to Broyles et al. ("Broyles '311") is presented as a second grounds of rejection to be reviewed on appeal.

The claims do not stand or fall together, but rather will be argued separately in accordance with the following groupings:

A. First Group of Claims: Claims 1-2, 6-7 and 19-20

B. Second Group of Claims: Claims 3-5

C. Third Group of Claims: Claims 8-13

D. Fourth Group of Claims: Claims 14-18

VII. ARGUMENT

A. PATENTABILITY OF FIRST GROUP CLAIMS 1-2, 6-7 AND 19-20

Independent claim 1 generally features steps of *"controlling an electrical load with a first code executed by a processor; releasing processor control so that the electrical load operates in an open control mode while the first code is displaced with a second code; and reinstating processor control of the electrical load using the second code."*

The obviousness rejection of claim 1 is improper including on the basis that neither Sato '776 nor Heydt '287 teach or suggest the "releasing" and "reinstating" steps, as well as on the basis that the skilled artisan would not find it desirable to arrive at the claimed combination from the cited references.

HEYDT '287 DOES NOT TEACH OR SUGGEST EITHER THE "RELEASING" OR "REINSTATING" OF PROCESSOR CONTROL AS SET FORTH BY CLAIM 1

A *prima facie* case of obviousness requires a showing that each of the claim limitations are actually taught or suggested by the prior art. *In re Royka*, 180 USPQ 580 (CCPA 1974); See also MPEP 2143.03; *In re Wilson*, 165 USPQ 494, 496 (CCPA 1970)(*All words in a claim must be considered in judging the patentability of that claim against the prior art*).

The Applicant agrees with the Examiner that Sato '776 fails to teach or suggest the "releasing" and the "reinstating" steps of claim 1. See non-final Office Action mailed October 12, 2007, page 3, lines 19-23. The Examiner errs, however, in asserting that Heydt '287 teaches or suggests these steps.

With regard to the teachings of Heydt '287, the Examiner stated:

> *Heydt teaches releasing processing control so that an electrical load operates in an open control mode (handoff control to motor control circuitry in a closed loop control mode, figure 5, paragraphs [0014] and [0016]). Heydt provides the advantage of a reliable means to accelerate a disk to an operational velocity (paragraph [0016]).* Office Action, page 4, lines 1-4 (emphasis added).

The Applicant respectfully submits that the reference by Heydt '287 to a "handoff" of control in a "closed loop control mode" does not mean, or even imply, that processor control is released and the electrical load operates in an open control mode.

Rather, Heydt '287 clearly teaches a number of closed loop control modes that are successively carried out by the motor control circuitry 132 under the continuous direction of the DSP processor 130, and no release of processor control takes place during any of these modes.

Heydt '287 specifically teaches as follows:

> *Early disc drive spindle motor designs used Hall effect or similar external sensors to provide an independent indication of motor positional orientation. However, present designs avoid such external sensors and instead use electronic commutation and back electromagnetic force (bemf) detection circuitry to provide closed-loop spindle motor control, such as disclosed by U.S. Patent No. 5,631,999 issued to Dinsmore.* Heydt '287, para [0007], lines 1-8 (emphasis added)

With regard to such bemf circuitry, Heydt '287 states as follows:

> *Above an intermediate operational speed, the* [bemf] *control circuitry will generally be able to reliably detect the bemf from rotation of the spindle motor, and will further be able to use the detected bemf to accelerate the motor to a final operational velocity. Below this intermediate speed, however, closed-loop motor speed control using detected bemf generally cannot be used since the spindle motor will not generate sufficient bemf at such lower speeds.* Heydt '287, para [0009], lines 1-8 (emphasis added)

It is clear from this that the reference to "closed-loop" motor speed control by Heydt '287 means closed-loop control *"using detected bemf."* From further review of the reference, the skilled artisan would conclude that the other modes of operation taught by Heydt '287 are also "closed loop" modes that are carried out by the motor control circuitry 132 of Heydt '287. These other closed-loop modes, however, do not rely on detected bemf.

The first mode taught by Heydt '287 is referred to as a "low gear mode" in which motor rotational position measurements and fixed length drive pulses are successively taken one after another. Each time a new commutation state of the motor is detected, the fixed length drive pulses are applied to the associated new set of windings appropriate for that commutation state. This sequence is graphically illustrated in FIG. 9 of Heydt '287. See paras [0011]-[0013], [0018], [0060]-[0062]. During low gear mode, multiple drive pulses and multiple measurements are made during each commutation state.

A "high gear mode" is switched in when the motor reaches a first intermediate velocity, such as around 250 rpm. Para [0051]. During high gear mode, variable length drive pulses are applied and calculations are performed to estimate when the next commutation transition state will likely be reached. As the next commutation state approaches, a currently applied drive pulse is terminated and measurements are sequentially initiated one after another to affirmatively detect this state transition. This sequence is graphically illustrated in FIG. 10 of Heydt '287. See paras [0019] and [0063]-[0065].

High gear mode continues until a second intermediate velocity is reached, such as around 1000 rpm. Para [0051]. A transition then takes place from the high gear mode to the so-called "*closed loop motor speed control using detected bemf.*" See para [0066]. This latter mode is used to complete the acceleration of the motor to the final desired velocity, such as about 15,000 rpm.

The Examiner focused on the use of the phrase "handoff" by Heydt '287 with regard to the transition from high gear mode to bemf detection mode control to assert that processor control is released. This is clearly without merit, as will now be shown.

The Examiner relied upon paras [0014] and [0066] of Heydt '287 in support of his position. Para [0014] appears in the background section of Heydt '287 and states as follows:

> *The final velocity achieved by this approach* [i.e., the "low gear mode"] *must be high enough* <u>*to enable a hand off*</u> *to the motor control circuitry; that is, the final velocity must be* <u>*high enough to enable the spindle motor to generate bemf that can be detected and used by the bemf detection circuitry*</u>*. However, the particular velocity at which bemf is reliably generated is a function of the motor contstruction, and recent generation high performance spindle motor designs with higher operational rotational velocities and fewer numbers of poles have been found to require a higher intermediate velocity before sufficient bemf is generated* <u>*to allow frequency lock by the motor control circuitry*</u>. Heydt '287, para [0014] (emphasis added).

Heydt '287 clearly explains what is meant by the phrase "*a hand off to the motor control circuitry*" in this section. Such "hand off" means activation of the bemf detection portion of the motor control circuitry to facilitate bemf detection based control. It most assuredly does not mean a hand off of control from a processor to motor control circuitry.

A review of para [0066] of Heydt '287 further supports this conclusion:

> *Once the spindle motor 106 reaches the intermediate velocity, the motor control circuitry 132 passes from the high gear mode to steady state (normal) closed-loop control mode. The resulting hand off in control is shown by passage of the routine from decision step 270 to step 272, wherein the motor control circuitry 132 acquires frequency lock from the bemf detection circuitry 138 and proceeds to accelerate the motor to the operational velocity (such as about 15,000 rpm). The routine then terminates at step 274.* Heydt '287, para [0066] (emphasis added)

This section also shows that the "*resulting hand off in control*" does not mean a hand off from the DSP processor 130 to the motor control circuitry 132, as postulated by the Examiner. Rather, the "*resulting hand off in control*" simply means activation of the bemf detection circuitry 138 within the motor control circuitry 132 to establish "*frequency lock*" so that the motor can be accelerated to the final velocity using the detected bemf.

Indeed, Heydt '287 explicitly states that "*the motor control circuitry 132 passes from the high gear mode to steady state (normal) closed-loop control mode.*" This directly contradicts the Examiner's characterization that the DSP processor 130 releases control during bemf detection mode to the motor control circuitry 132.

With this understanding of the teachings and suggestions of Heydt '287, it can now be readily seen that Heydt '287 fails to teach or suggest a step of "*releasing processor control so that the electrical load operates in an open control mode while the first code is displaced with a second code*," as featured by claim 1.

No "releasing of processor control" takes place during any of the control modes of FIG. 5. Rather, as with Sato '776, a continual passage of commands and state data are exchanged between the DSP processor 130 and the motor control circuitry 132 during the operation of the routine of FIG. 5 in Heydt '287. See FIGS. 2-3 and para [0041], lines 1-4. The DSP 130 actively monitors the acceleration of the motor, and signals to the control logic portion 134 of the motor control circuitry 132 when to transition to each of the low gear, high gear and bemf detection based modes, as well as when to terminate the routine once the final velocity is reached.

Moreover, Heydt '287 is wholly silent with regard to teaching or suggesting the releasing of processor control so that the motor operates in an "*open control mode*" while "*the first code is <u>displaced</u> with a second code*." The steps of FIG. 5 correspond to a single programming routine enacted by the DSP 130. Nothing in FIG. 5, or anywhere else in Heydt '287, can be remotely viewed as a second code which displaces a first code as claimed.

Heydt '287 thus further fails to teach or suggest "*reinstating processor control of the electrical load using the second code*" as further featured by claim 1. There is no "*second code,*" and there is no "*reinstating of processor control*" at all.

For these reasons, reliance upon Heydt '287 by the Examiner is misplaced. No *prima facie* case of obviousness has been made, and the Board is respectfully requested to reverse the rejection of claim 1, as well as for the claims depending therefrom.

THE SKILLED ARTISAN WOULD NOT FIND IT DESIRABLE TO ARRIVE AT THE SUBJECT MATTER OF CLAIM 1 FROM THE CITED REFERENCES

As the Board will appreciate, the Supreme Court has recently clarified the law with regard to obviousness determinations. See *KSR International Co. v. Teleflex Inc.*, 82

USPQ2d 1385 (2007). In *KSR*, the Court rejected a rigid application of the so-called teaching-suggestion-motivation (TSM) test in favor of a more flexible approach to the inquiry based on the factors set forth by *Graham v. John Deere*, 363 US 1 (1966). Generally, the so-called teaching-suggestion-motivation (TSM) test is still available for use, so long as it is not rigidly applied in a formulistic sense. KSR at 1399.

In all cases, the obviousness determination cannot be based on merely conclusory statements by the Examiner; rather, there must be "*some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness.*" *KSR at* 1396, quoting *In re Kahn*, 78 USPQ2d 1329 (Fed. Cir. 2006).

The Examiner justified the combination of Sato '776 and Heydt '287 as follows:

> *It would have been obvious to the one of ordinary skill in the art, having the teachings of Sato and Heydt before them at the time the invention was made to <u>modify the system of Sato</u> to use the <u>closed loop spindle motor acceleration control of Heydt</u> to achieve and maintain the rotation speeds of the disk in Sato. This modification would result in <u>releasing processor control</u> so that the electrical load would operate in an <u>open control mode</u> while the first code is <u>displaced</u> with the second control and would result in <u>reinstating</u> control of the electrical load using the second code.* Office Action, page 4, lines 5-10 (emphasis added)

The Examiner's statement that the claimed combination would result from the modification of the system of Sato '776 with the acceleration control of Heydt '287 is wholly without merit. The Examiner posits that such combination would result in "*<u>releasing processor control</u> so that the electrical load would operate in an <u>open control mode</u> while the first code is <u>displaced</u> with the second control and would result in <u>reinstating</u> control of the electrical load using the second code.*" This is a surprising result, inasmuch as neither reference teaches or suggests this individually.

The Examiner has correctly admitted that there is no releasing of processor control in Sato '776, there is no operation of an electrical load in an open control mode while first code is displaced with second code in Sato '776, and there is no reinstating of processor control using the second code in Sato '776.

This is true for Heydt '287 as well. There is no releasing of processor control in Heydt '287; there is no operation of an electrical load in an open control mode while first code is displaced with second code in Heydt '287; and there is no reinstating of processor control using the second code in Heydt '287. Rather, as in Sato '776, the DSP processor 130 in Heydt '287 continuously monitors and directs the operation of the motor control circuitry 132 throughout the entire acceleration operation. See FIG. 5 and paras [0050]-[0052], [0063] and [0066].

Substitution of the acceleration control of Heydt '287 into the system of Sato '776 would not result in the actual subject matter that is claimed by claim 1. The Examiner may be right that such substitution would provide better, faster and more reliable acceleration. But achieving better, faster, or more reliable acceleration is not enough to show how the combination results in the particular language of claim 1.

At least the Examiner cannot be accused of engaging in improper hindsight reconstruction per *Graham*, such this requires the Examiner to have actually found the constituent elements of the claim in the prior art. Instead, the Examiner is guilty of mischaracterizing the teachings and suggestions of the Heydt '287 reference. Such mischaracterization prevents the rejection from being based on articulated reasoning with the requisite "*rational*" underpinning. *KSR, Supra.*

The Examiner further justified the rejection as follows:

> *One of ordinary skill in the art would have been motivated to make this modification in order to reliably accelerate the disk of Sato in view of Heydt. Further, by handing off the acceleration of the disk to a motor driver controller, it would allow the processor would be able to processor other information.* Office Action, page 4, lines 11-14 (emphasis added).

The Examiner is incorrect in stating that Heydt '287 teaches or suggests to hand off the acceleration of the motor by the processor (DSP 130) to a motor driver controller (circuitry 132). Office Action, page 4, lines 13-15. As noted above, the motor control circuitry 132 seamlessly transitions from one mode (e.g., high gear) to another mode (e.g., bemf detection based control) based on continuously applied processor control by the DSP 130.

Moreover, surmising that the DSP 130 would somehow release control so that it could "process other information in the meantime," as suggested by the Examiner, gets the skilled artisan no closer to the claimed invention. There is no processing of other information in the meantime since the DSP 130 is busy executing the routine of FIG. 5. But even if the DSP 130 turned away from the task at hand to "process other information in the meantime," the Applicant still wonders why this would teach or suggest displacement of the first code with a second code, as claimed. The Examiner does not say.

Finally, for good measure the Examiner threw in the "predicable results" rationale from *KSR* to justify the combination of Sato '776 and Heydt '287, as follows:

> *Also, because both Sato and Heydt teach methods of accelerating a disk to operational speeds it would have been obvious to one of ordinary skill in the art to substitute the method of Heydt for the method used by Sato to achieve the predictable result of accelerating the disk to an operational speed.* Office Action, page 4, lines 14-17 (emphasis added).

The Examiner appears to have misapprehended what the Court meant in *KSR* when referring to "predictable results." Specifically, the Court stated that "a court must ask whether the improvement is more than the predictable use of prior art elements according to their established functions." *KSR at 1389* (emphasis added). In such a case, "a combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results." *KSR, Supra* (emphasis added).

That is not the case here. The question is not whether the respective teachings of Heydt '287 and Sato '776 could be combined in such a way as to accelerate a motor in a predictable way, but rather, whether such teachings would accelerate a motor in the manner claimed. Since the Applicant has amply demonstrated that the various "releasing" and "reinstating" steps of claim 1 are not merely "familiar elements" well known in the art, the "predictable results" test is not applicable. Indeed, the absence of such elements from the references is a strong indicator that the claimed combination is in fact patentable.

In sum, the rejection is based on a blatant mischaracterization of Heydt '287. It is clear error for the Examiner to assert that the Heydt '287 teaches a handoff of control from a processor to the motor control circuitry 132 when bemf based detection is initiated. There is absolutely nothing in Heydt '287 (or in Sato '776) that even remotely suggests this takes place. There is further absolutely nothing in Heydt '287 (or in Sato '776) that even remotely suggests such a release of processor control takes place so that a first code is displaced with a second code, as claimed.

For these reasons, the rejection is improper, and the Board is requested to reverse the rejection of the claim.

B. PATENTABILITY OF SECOND GROUP CLAIMS 3-5

Dependent claims 3-5 depend from claim 1, and were rejected under §103(a) as obvious over Sato '776 and Heydt '287, further in view of Broyles '311. These claims are argued separately because of the different basis for rejection. The dependent claims 3-5 are submitted as being patentable as depending from a patentable base claim, and reconsideration and withdrawal of the §103(a) rejection of these claims are requested on this basis.

C. PATENTABILITY OF THIRD GROUP CLAIMS 8-13

Independent claim 8 generally features "*using a processor to <u>execute startup code</u> loaded into a memory location to <u>initiate operational control</u> of an electrical load; <u>continuing to operate</u> the electrical load while <u>processor operational control</u> of the electrical load <u>is temporarily suspended</u> to <u>load application code</u> to the memory location; and <u>resuming operational control</u> of the electrical load <u>using the application code</u>.*"

Claim 8 stands finally rejected as being obvious over Sato '776 and Heydt '287, further in view of Broyles '311. This is respectfully traversed on the following bases.

THE CITED REFERENCES AT LEAST FAIL TO TEACH OR SUGGEST THE "TEMPORARY SUSPENDED" LANGUAGE OF CLAIM 8

The various teachings and suggestions of Sato '776 and Heydt '287 have been discussed at length above, and so will not be repeated here. A review of Broyles '311 has already been provided in the previously filed Appeal Brief, and so only a brief synopsis will be supplied now.

Broyles '311 generally teaches a nonvolatile memory (flash ROM 78) with a revision indicator that maintains a revision level for hardware present in a computer system S. See FIGS. 1-2, col. 3, lines 21-35; col. 5, lines 59-65. The revision indicator may be referenced during a powerup sequence in which a BIOS boot program is executed, followed by a system level operating system (OS). See FIG. 5. Broyles '311 further teaches to move the contents of the ROM 78 to an NVRAM security device 80 accessible only by the BIOS and the OS. Col. 7, lines 10-25.

Nothing in Sato '776, Heydt '287 or Broyles '311 remotely suggests "*continuing to operate* the electrical load while *processor operational control* of the electrical load *is temporarily suspended* to *load application code* to the memory location," as featured by claim 8.

Sato '776 uses a branch instruction to switch from the boot program to the main program. Heydt '287 uses a single set of code as illustrated by FIG. 5 therein to transition through the low gear, high gear and bemf detection modes of acceleration control. Broyles '311 maintains a record of what hardware is present for use by a boot program and an operating system in turn.

The Examiner, however, maintains that Heydt '287 does in fact carry out the "continuing to operate" step of claim 8, as modified by the "memory location" supplied by Broyles '311. More specifically, the Examiner stated:

> *Regarding claims 3-5, 8-13, Sato together with Heydt and Broyles taught the claimed apparatus* [of independent claim 14], *therefore together they teach the claimed method* [of independent claim 8]. Office Action, page 9, lines 9-10 (emphasis added)

Initially, the Applicant notes that the language of independent apparatus claim 14 is different from the language of claim 8. For example, claim 8 does not recite operation of the electrical load in an open control mode. Nevertheless, the foregoing statement by the Examiner will be interpreted as meaning that the references are being applied to claims 8 and 14 in the same way.

With regard to the rejection of claim 14, the Examiner stated:

> *Heydt teaches an electric load (disk 108) and temporarily releasing operational control of the electric load such that the electric load to operates in an open control mode (handoff control to motor control circuitry in a closed loop control mode, figure 5, paragraphs [0014] and [0066]).* Office Action, page 6, lines 18-22 (emphasis added).

> *Broyles teaches wherein startup code is loaded in a memory location (wherein the startup codes is the "boot code" and the memory location is a "RAM" col. 6, lines 58-65).* Office Action, page 7, lines 16-17 (emphasis added)

The Applicant interprets this to mean that Heydt '287 is being relied upon to teach "*processor operational control of the electrical load is temporarily suspended,*" and Broyles '311 additionally supplies the language "*to load application code to the memory location.*" This is respectfully traversed.

It is inconsistent for the Examiner to take the position that Sato '766 does not temporarily suspend processor operational control, but Heydt '287 does. As previously noted by the Applicant in the prior Appeal Brief (see pp. 15-16), the claim term "operational control" is defined in the specification of the present application as a mode "*whereby the processor engages in continual active regulation, intervention or verification to maintain the continued operation of the load, or simply a mode where the processor controls the load.*" Specification, page 16, lines 22-25.

To "temporarily suspend" such operational control would require a cessation of such regulation, intervention, verification or control. This is supported, for example, in the specification at page 10, lines 16-23.

But a review of Heydt '287 shows no cessation of the continued active regulation, intervention or verification of the acceleration process by the DSP 130 as carried out by the motor control circuitry 132. FIG. 5 of Heydt '287 shows such transitions to take place at decision steps 252 and 270, respectively.

With regard to the transition at step 252, Heydt '287 states as follows:

> *Once the spindle motor 106 reaches the first velocity, such as around 250 rpm, the routine transitions to the high gear mode, as indicated by decision step 256 in FIG. 5.* Heydt '287, para [0063], lines 1-4 (emphasis added)

The skilled artisan would not view the language "*the routine transitions to the high gear mode*" as explicitly or inherently meaning that processor operational control is temporarily suspended in any way, shape or form. Indeed, since the judgment is made to transition based on the monitored motor velocity (i.e., the motor speed reaches a level around 250 rpm), the skilled artisan would view the DSP processor 130 as being actively involved in making this decision to switch to high gear. Thus, continual processor control is maintained, just as it is in Sato '776.

With regard to the transition at step 270 from high gear to bemf detection control, Heydt '287 states as follows:

> *Once the spindle motor 106 reaches the intermediate velocity, the motor control circuitry 132 passes from the high gear mode to steady-state (normal) closed-loop control mode. The resulting hand off in control is shown by passage of the routine from decision step 270 to 272, wherein the motor control circuitry 132 acquires frequency lock from the bemf detection circuitry 138 and proceeds to accelerate the motor to the operational velocity*

(such as about 15,000 rpm). The routine then terminates at step 274. Heydt '287, para [0066], lines 1-9 (emphasis added)

As noted above, there is absolutely nothing in Heydt '287 that can be remotely viewed as supporting an interpretation that the "resulting hand off in control" means operational control is released by the DSP 130 and passed to the motor control circuitry 132. Rather, the "hand off in control" means that the bemf detection circuitry 138 of the motor control circuitry 132 is now activated, whereas before it was not.

The DSP processor 130 maintains continued active monitoring during this time, first by signaling to the control logic block 134 (FIG. 3) that it is time to enact bemf based control, and then by continuing to monitor the acceleration of the motor to the operational velocity and signaling when the acceleration process is complete. It is only in the Examiner's imagination that the DSP processor 130 takes a dirt nap and releases operational control when bemf detection mode is initiated. Heydt '287 certainly does not teach this.

Heydt '287 therefore fails to teach or suggest a temporary suspension of processor operational control, as claimed. Indeed, it is even less likely that Heydt '287 carries out such suspension than Sato '776; at least in Sato '776 a branch instruction is executed to pass from the boot program to the main program. Heydt '287 does not even teach that, and instead uses a single set of code for the entire acceleration process.

Similarly, the movement of boot programming from a ROM to a RAM, as taught by Broyles '311, adds nothing with regard to "temporarily suspending processor operational control" as claimed by claim 8. Reversal of the rejection of claim 8, and for the claims depending therefrom, are respectfully requested on this basis.

THERE IS NOTHING IN THE CITED REFERENCES THAT WOULD SUGGEST THE DESIRABILITY, AND THUS THE OBVIOUSNESS, OF MODIFYING THE REFERENCES TO ARRIVE AT THE SUBJECT MATTER OF CLAIM 8

As mandated by *Graham,* an obviousness determination by the Office requires the claimed invention to be considered as a whole, the references must be considered as a whole and must suggest the desirability and thus the obviousness of making the combination, the references must be viewed without the benefit of impermissible hindsight vision afforded by the claimed invention; and a reasonable expectation of success must be shown. See MPEP 2141.

With regard to the claimed subject matter of claim 8, there is nothing in Sato '776, Heydt '287 or Broyles '311, alone or in combination, that would suggest the desirability of modifying and/or combining these references to arrive at the claimed subject matter.

Simply put, none of the various references teach or suggest "*continuing to operate the electrical load while processor operational control of the electrical load is temporarily suspended to load application code to the memory location.*" As none of the references even suggest such operation, it cannot be reasonably concluded that the skilled artisan would find it desirable to implement such operation.

Reversal of the rejection of claim 8, and for the claims depending therefrom, are accordingly solicited.

D. PATENTABILITY OF FOURTH GROUP CLAIMS 14-18

Independent claim 14 generally features "*a programmable processor*" which "*executes startup code loaded into the memory location to initiate operational control of the load, temporarily releases operational control of the electrical load so that the electrical*

load continues to operate in an *<u>open control mode</u>* *while application code is loaded to the memory location, and* *<u>resumes operational control</u>* *of the electrical load using the application code."*

As with claims 8-13, the Applicant respectfully submits that no *prima facie* case of obviousness of independent claim 14 has been established by the Examiner in view of Sato '776, Heydt '287 and Broyles '311.

THERE IS NOTHING IN THE CITED REFERENCES THAT WOULD SUGGEST THE DESIRABILITY, AND THUS THE OBVIOUSNESS, OF MODIFYING THE REFERENCES TO ARRIVE AT THE SUBJECT MATTER OF CLAIM 14

When considering the claimed subject matter of claim 14 as a whole (per *Graham*), the skilled artisan would note that claim 14 generally includes a processor which "*<u>temporarily releases operational control</u>* *of the electrical load so that the electrical load continues to operate in an* *<u>open control mode while application code is loaded</u>* *to the memory location."*

The skilled artisan would find this language of claim 14 to include a temporary release of "*operational control*," and an operation of the load in "*open control mode*," while the "*application code is loaded to the memory location.*" These respective claim terms would be understood as discussed above.

When considering Sato '776 as a whole (per *Graham*), it can be readily seen that the transfer of the main program from disk to RAM 414 is carried out under the direction of the <u>program loading section 417</u> of processor 412. See FIG. 3, and para [0088]. As noted above, there is nothing that could be reasonably construed from Sato '776 to indicate that the processor 412 maintains constant control with the disk monitoring section 411 sufficient to

transfer the main program from disk, while *at the same time* releasing operational control of the spindle motor 404 during this transfer.

Rather, the express teachings at para [0006] *et seq.* of continual data exchanges between the disk monitoring section 411 and the processor 412 would indicate to the skilled artisan that operational control of the spindle motor 404 is also maintained by the processor 412 during this data transfer sequence.

Thus, when considering Sato ‘776 as a whole, continual active operational control is maintained during the loading of the main program, which is directly contrary to the language of claim 14. It is believed this would generally tend to weigh against a finding of “desirability to modify/combine” the Sato ‘776 reference.

The DSP processor 130 in Heydt ‘287 operates in a similar fashion to the processor of Sato ‘776, in that the DSP processor 130 continuously directs the various low gear, high gear and bemf detection based modes of FIG. 5. Nothing in Heydt ‘287 indicates otherwise, and thus there is nothing that substantiates the Examiner’s unsupported allegations that Heydt ‘287 teaches to temporarily release operational control of the load.

Accordingly, there is nothing in Sato ‘766, in Broyles ‘311, or in the art in general, that would suggest the desirability of modifying and/or combining the references to arrive at the system as claimed by claim 14, as required to establish a *prima facie* case of obviousness.

Conclusion

For the foregoing reasons, the Applicant respectfully submits that claims 1-20 define subject matter that is patentable over the art of record, and respectfully requests that the Board reverse the final rejection of claims 1-20.

Respectfully submitted,

By: ______________________

Randall K. McCarthy, Reg. No. 39,297
Fellers, Snider, Blankenship, Bailey & Tippens
100 North Broadway, Suite 1700
Oklahoma City, Oklahoma 73102
Telephone: (405) 232-0621
Facsimile: (405) 232-9659
Customer No. 33900

VIII. CLAIMS APPENDIX

1. (Original) A method, comprising:

controlling an electrical load with a first code executed by a processor;

releasing processor control so that the electrical load operates in an open control mode while the first code is displaced with a second code; and

reinstating processor control of the electrical load using the second code.

2. (Original) The method of claim 1, wherein the first code of the controlling step is supplied from a boot read only memory (ROM).

3. (Original) The method of claim 1, wherein the controlling step comprises loading the first code into a first memory location accessed by the processor.

4. (Original) The method of claim 3, wherein the controlling step further comprises loading the second code into a second memory location accessible by the processor.

5. (Original) The method of claim 4, wherein the releasing step comprises moving the second code from the second memory location into the first memory location, thereby displacing the first code from the first memory location.

6. (Original) The method of claim 1, wherein the electrical load is a motor.

7. (Original) The method of claim 6, wherein the motor supports a data storage medium, and wherein the controlling step comprises using the motor to rotate the data storage medium at an operational velocity and retrieving the second code from the rotating data storage medium.

8. (Previously presented) A method, comprising:

using a processor to execute startup code loaded into a memory location to initiate operational control of an electrical load;

continuing to operate the electrical load while processor operational control of the electrical load is temporarily suspended to load application code to the memory location; and

resuming operational control of the electrical load using the application code.

9. (Original) The method of claim 8, wherein the startup code of the using step is supplied from a boot read only memory (ROM).

10. (Original) The method of claim 8, wherein the memory location of the using step is characterized as a first memory location, and wherein the using step further comprises loading the application code into a second memory location accessible by the processor.

11. (Original) The method of claim 10, wherein the continuing step comprises moving the application code from the second memory location into the first memory location, thereby displacing the startup code from the first memory location.

12. (Original) The method of claim 8, wherein the electrical load comprises a motor supporting a data storage medium, and wherein the using step comprises energizing the motor to rotate the data storage medium at an operational velocity and retrieving the application code from the rotating data storage medium.

13. (Original) The method of claim 12, wherein the using step further comprises using the startup code to energize an actuator motor to bring a data transducing head into alignment with a track defined on the data storage medium, and utilizing the head to transduce the application data from said track.

14. (Previously presented) An apparatus, comprising:

an electrical load;

a memory location; and

a programmable processor coupled to the memory location and adapted to control the electrical load, wherein during an initialization process the processor executes startup code loaded into the memory location to initiate operational control of the load, temporarily releases operational control of the electrical load so that the electrical load continues to operate in an open control mode while application code is loaded to the memory location, and resumes operational control of the electrical load using the application code.

15. (Original) The apparatus of claim 14, further comprising a boot read only memory (ROM) which stores the startup code, wherein the startup code is loaded from the boot ROM to the memory location for execution by the processor.

16. (Original) The apparatus of claim 14, wherein the memory location of the using step is characterized as a first memory location, and wherein the apparatus further comprises a second memory location accessible by the processor and into which the processor loads the application code.

17. (Original) The apparatus of claim 14, wherein the electrical load comprises a motor supporting a data storage medium, and wherein the execution of the startup code by the processor results in the energizing of the motor to rotate the data storage medium at an operational velocity.

18. (Original) The apparatus of claim 17, further comprising an actuator motor coupled to a data transducing head, and wherein the execution of the startup code by the processor further results in the energizing of the actuator motor to bring the head into alignment with a track defined on the data storage medium, the head transducing the application data from said track.

19. (Previously presented) The method of claim 1 wherein the processor operationally controls the electrical load.

20. (Previously presented) The method of claim 1, wherein at least one control signal is applied to the electrical load during the open control mode of the releasing step.

IX. EVIDENCE APPENDIX

No additional evidence is included.

X. RELATED PROCEEDINGS APPENDIX

There exist no relevant related proceedings concerning this Appeal before the Board.